1. A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixels in a second column; and

an operational amplifier-based charge sensing circuit, associated with only the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit.

2. The circuit of claim 1 further including an array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit.

3. The circuit of claim 1 further including:

a first array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit with respect to signals sampled by the first sample-and-hold circuit; and

a second array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit with respect to signals sampled by the second sample-and-hold circuit.

4. The circuit of claim 1 wherein a pre-gain offset voltage selectively can be added to a signal sampled by one of the sample-and-hold circuits.

5. The circuit of claim 1 wherein the operational amplifier-based charge sensing circuit includes a switched capacitor integrator.

6. A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a sample-and-hold circuit for sampling and storing signals from sensors in a single column of pixels in the array; and

an operational amplifier-based charge sensing circuit, associated with only the single column in the array, that provides an amplified differential output signal based on signals sampled by the sample-and-hold circuit.

7. The circuit of claim 6 further including an array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit.

8. A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixels in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique.

9. The circuit of claim 8 wherein the operational amplifier-based charge sensing circuit includes a switched capacitor integrator.

10. The circuit of claim 8 wherein the analog-to-digital converter includes a comparator and a first binary-scaled capacitor network, wherein the capacitors in the first network share a common node coupled to a first input of the comparator, and wherein the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator.

11. The circuit of claim 10 wherein each of the capacitors in the first capacitor network has an associated latch circuit for storing a bit corresponding to a differential signal for a pixel sampled by the first sample-and-hold circuit while a differential signal for a pixel sampled by the second sample-and-hold circuit is amplified and converted to a corresponding digital signal.

12. The circuit of claim 10 further including:

a calibration network for providing a signal to cancel an offset of the comparator.

13. The circuit of claim 12 further including:

a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator, wherein the capacitors in the second capacitor

network share a node in common with the capacitors in the first capacitor network.

14. The circuit of claim 13 wherein the calibration network selectively can be enabled to provide a DC shift to the common node to ensure that the signal for cancelling the comparator offset appears as a positive voltage.

15. The circuit of claim 13 wherein one side of each capacitor in the first capacitor network selectively can be connected to a first reference voltage, and wherein one side of each capacitor in the second capacitor network selectively can be connected to a second reference voltage different from the first reference voltage.

16. The circuit of claim 13 wherein the calibration network selectively can be enabled to provide a post-gain offset for the differential output signal from the charge sensing circuit.

17. A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a sample-and-hold circuit for sampling and storing signals from sensors in a single column of pixels in the array;

an operational amplifier-based charge sensing circuit, associated with only the single column, that provides an amplified differential output signal based on signals sampled by the sample-and-hold circuit; and

an analog-to-digital converter, associated only with only the single column, for converting the differential output to a corresponding digital signal using a successive approximation technique.

18. A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each circuit includes:

a first sample-and-hold circuit for sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit for sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique.

19. The imager of claim 18 wherein each readout circuit further includes an array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit.

20. The imager of claim 18 wherein each readout circuit further includes:

a first array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit with respect to signals sampled by the first sample-and-hold circuit; and

a second array of capacitors which selectively can be enabled to choose a gain associated with the operational amplifier-based charge sensing circuit with respect to signals sampled by the second sample-and-hold circuit.

21. The imager of claim 18 wherein, for each readout circuit, a pre-gain offset voltage selectively can be added to a signal sampled by one of the sample-and-hold circuits.

22. The imager of claim 18 wherein, for each readout circuit, the operational amplifier-based charge sensing circuit includes a switched capacitor integrator.

23. The imager of claim 18 wherein, for each readout circuit, the analog-to-digital converter includes a comparator and a first binary-scaled capacitor network, wherein the capacitors in the first network share a common node coupled to a first input of the comparator, and wherein the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator.

24. The imager of claim 23 wherein, for each readout circuit, each of the capacitors in the first capacitor network has an associated latch circuit for storing a bit corresponding to a differential signal for a pixel sampled by the first sample-and-hold circuit while a differential signal for a pixel sampled by the second sample-and-hold circuit is amplified and converted to a corresponding digital signal.

25. The imager of claim 24 wherein the latch circuits in each readout circuit also can store bits corresponding to a differential signal for a pixel sampled by a respective one of the second sample-and-hold circuits, wherein the imager further includes a bus, and wherein the latch circuits in a particular readout circuit selectively can be enabled to transfer the bits to the bus.

26. The imager of claim 23 wherein each readout circuit further includes:

a calibration network for providing a signal to cancel an offset of the comparator.

27. The imager of claim 26 wherein each readout circuit further includes:

a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator, wherein the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network.

28. The imager of claim 27 wherein, for each readout circuit, the calibration network selectively can be enabled to provide a voltage shift to the common node to ensure that the signal for cancelling the comparator offset appears as a positive voltage.

29. The imager of claim 27 wherein, for each readout circuit, one side of each capacitor in the first capacitor network selectively can be connected to a first reference voltage, and wherein one side of each capacitor in the second capacitor network selectively can be connected to a second reference voltage different from the first reference voltage.

30. The imager of claim 27 wherein, for each readout circuit, the calibration network selectively can be enabled to provide a post-gain offset for the differential output signal from the charge sensing circuit.

31. A method of reading out values from active pixel sensors in an array of sensors, wherein the array includes rows and columns of sensors, the method comprising:

selecting a row of sensors whose values are to be read out;

sampling signal and reset levels for two sensors in the selected row;

providing a differential output signal based on the sampled signals for a selected one of the sensors using an operational amplifier-based charge sensing circuit associated with only the two columns in which the two sensors are located;

converting the differential output signal to a corresponding digital signal using an analog-to-digital converter associated with only the two columns.

32. The method of claim 31 further including providing a pre-gain offset voltage to a sampled signal.

33. The method of claim 31 further including selecting a gain for the differential output signal.

34. The method of claim 31 wherein the act of converting includes using a successive approximation technique.

35. The method of claim 31 wherein the act of converting includes providing a signal to cancel a comparator offset.

36. The method of claim 35 wherein the act of converting further includes providing a DC voltage shift to ensure that the signal for cancelling the comparator offset appears as a positive voltage.

37. The method of claim 31 further including providing a post-gain offset for the differential output signal.